



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,993	08/30/2001	Anthony Moschopoulos	703.155US1	1856
21186 7590 02/27/2007 SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402			EXAMINER CHOI, WOO H	
			ART UNIT	PAPER NUMBER
			2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/944,993	MOSCHOPOULOS, ANTHONY	
	Examiner	Art Unit	
	Woo H. Choi	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 November 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-46 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-46 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 5, 7 – 9, 13 – 18, 21, 23 and 25 – 27 are rejected under 35 U.S.C. 102(e) as being anticipated by de la Iglesia *et al.* (US Patent No. 6,490,703, hereinafter “de la Iglesia”).
3. With respect to claims 1, 13 and 17 de la Iglesia discloses a method of transferring a data stream (figure 8) comprising:

directly transferring a plurality of bits associated with a data stream from an external data source device (figure 5, processor 304 is a device that is different from the memory interface and memory, see also figure 8, step 808) to a temporary storage associated with a different device (figure 5, memory 306 and its associated interfaces 400, 144, figure 8, step 818), wherein each device includes its own storage and processing capabilities (CPU has its own storage, for example, registers and program counters; and the memory and its interface combination has its own processing capability to generate and decode ECC and to process inversions);

concurrently intercepting during the transfer each bit associated with the data stream and counting a bit-transfer total and a bit-set total associated with the data stream (figure 8, step 810); and

determining if the bit-set total exceeds more than half the bit-transfer total (steps 810, col. 9 lines 26 – 31) and if so setting an inversion flag bit which is associated with the data stream (step 816, see also figure 2 and col. 14 – 27, flip bits indicate the state of data inversion) and wherein the processing of the method and the temporary storage reside with a same controller as one another (figure 5, the source, the method and the temporary storage all reside in the same computer or a controller).

4. With respect to claim 2 and 18 the method further comprises:

transferring from the temporary storage to a target source each bit associated with the data stream and concurrently inverting each bit as transferred, if the inversion flag bit is set (steps 818 – 828, if the bits stored in the memory 306 are inverted in step 814, they are recovered in step 826 by inverting again).

5. With respect to claim 3, the method further comprises:

shifting the inversion flag bit to a flag storage (818, flag bits are stored or “shifted” to memory).

6. With respect to claims 4 and 14, the method further comprises:

assembling one or more additional inversion flag bits in the flag storage, each additional inversion flag bit associated with a single additional data stream; and

maintaining each additional data stream in the temporary storage (figure 8, the process of data word inversion determination and the storage of an inverted data word with flip bits occurs for every 64 bit data word with memory storing a plurality of data words with the associated flip bits).

7. With respect to claim 5, 15 and 16, the method further comprises:

transferring from the temporary storage to a target source each bit associated with the data stream and each of the additional data streams while concurrently inverting each transferred bit, if the inversion flag bit associated with a transferred data stream is set, as identified in the flag storage (steps 818 – 828, see rejection of claim 2 above).

8. With respect to claims 7 and 21, de la Iglesia discloses a method of transferring a data stream (figure 8), comprising:

receiving a data stream and an inversion flag associated with the data stream from an external data source into a different device (processor is device that is different an external to memory interface and memory);

transferring one or more bits associated with the data stream from a data source to a target source, if the inversion flag is unset; and

inverting, on or within the data source (figure 5, 304, 400), the bits associated with the data stream as the data stream is transferred from the data source to the target source, if the inversion flag is set (steps 820 – 828).

9. With respect to claim 8 the inversion flag and the data stream are stored together in the data source (step 818, flop bits and data are both stored in the memory).

10. With respect to claim 9 the inversion flag and the data stream are separately stored in the data source (flip bits and data occupy separate spaces in the memory).

11. With respect to claim 23, the controller acquires the inversion bit by stripping the inversion bit from the data stream (figure 8, steps 818 – 824).

12. With respect to claim 25, de la Iglesia discloses system for transferring a data stream, comprising:

a control buffer (figure 5, 304, processor registers and other processor storage resources);

a storage buffer (306);

an inversion storage (306, memory stores data as well as inversion bits);

a counting set of executable instructions to count set bits associated with a data stream being received from the control buffer directly into the storage buffer (data stream flows from the processor directly into the memory through the memory interface without passing through any other devices, the Examiner notes that although not disclosed by Applicant, interface circuits

Art Unit: 2189

are required to transfer data between devices), wherein the control buffer is an external data source to the storage buffer (processor 305 is external to the memory system), and the counting set of executable instructions generates an inversion bit associated with the data stream, wherein the inversion bit is housed in the inversion storage and is set if a total number of set bits exceeds more than half a total number of bits associated with the data stream (figure 8, 810), and wherein the counting set of instructions, the inversion storage, and the storage buffer are included within a same controller (figure 5, these are include included in the memory system 400 + 114 + 306) and the device that is different from another device associate with the control buffer that supplies the data stream (figure 5, 300).

13. With respect to claim 26, the system further comprises:

a transfer set of executable instructions operable to use the counting set of executable instructions to transfer the data stream from the storage buffer to a target device, wherein the entire data stream is inverted if the inversion bit is set as the data stream is being transferred to the target device (824 – 828).

14. With respect to claim 27, the inversion bit is transferred with the data stream to the target device (816).

15. Claims 1 – 37, 39 – 41 and 44 – 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Norman (US Patent No. 5,873,112).

With respect to claims 7, 11, 12, 21, 28, 32, 33 and 36, Norman discloses a method of transferring a data stream, comprising:

directly receiving a data stream (see figure 7) and an inversion flag (col. 18, lines 30 – 33) associated with the data stream from an external data source device (figure 7, host processor 401) into a different device (figure 7, 429 and 416), wherein each device includes its own storage and processing capabilities (the host processor as a minimum has, registers and the controller and the memory combination has inversion processing capability);

transferring one or more bits associated with the data stream from a external data source device to a target source (figure 7, 401), if the inversion flag is unset; and

inverting, on or with the data source, the bits associated with the data stream as the data stream is transferred from the external data source device to the target source, if the inversion flag is set (col. 18, lines 46 – 56), wherein the data stream is processed and temporarily housed in storage (figure 3, 104) within a same controller as it is transferred to the target source.

16. With respect to claims 8, 23, 27 and 30, the inversion flag and the data stream are stored together in the data source (polarity bits or inversion flags are stored in the flash array).

17. With respect to claims 9 and 24, inversion flag and the data stream are separately stored in the data source (col. 18, lines 30 – 33, polarity bits for an entire sector are stored separately from the actual data sector).

18. With respect to claim 10, the inversion flag is stored with one or more additional inversion flags as a single data structure in the data source, each additional inversion flag associated with an additional data stream (see rejection of claim 9 above, polarity bits are for an entire sector are stored together with one bit representing one data packet).
19. With respect to claim 22, the system further comprises:
 - a temporary storage (figure 3, 104) operable to house the data stream as the data stream is acquired from the data source device; and
 - a register storage (figure 3, 118) operable to house the inversion bit as the data stream is acquired from the data source device.
20. With respect to claim 29 – 31, and 34, the apparatus further comprises:
 - a buffer (figure 3, 104) to house the packet prior to transfer; and
 - a register (118) to house the inversion bit.
21. With respect to claim 35, the state machine is configured by interfacing one or more electro-mechanical devices (216 and other circuits, see page 3 of the specification, Applicant seems to regard any semiconductor type of devices to be electro-mechanical devices).
22. With respect to claim 37, the data packet is a fixed length data packet (figure 2).
23. With respect to claim 39, the apparatus is a flash memory device (figure 3, 216).

24. With respect to claims 1, 13, 17, 19, Norman discloses an inversion data transfer system (figure 7), comprising:

an external data source device (401 or 416);

a temporary storage associated with a different device from that of the external data source device (figure 3, 104); and

a controller (429) that directly transfers a data stream having a plurality of bits from the data source device to the temporary storage, and concurrent to the transfer determines if a total number of set bits within the data stream is more than half of a total number of bits associated with the data stream, and if so associating a set inversion bit with the data stream, otherwise associating an unset inversion bit with the data stream (see also abstract and claim 1, and discussions related to figure 3) wherein the temporary storage resides within the controller and on the same device as the temporary storage and separate from the external data source device (figure 3, 104 resides in chip 3); and

a register storage operable to house the inversion bit and one or more additional inversion bits, wherein each additional inversion bit is associated with an additional data stream (figure 3, 118, col. 15, lines 65 – 67 and col. 17, lines 50 – 54).

25. With respect to claims 2 – 6, 14 – 16 and 20, the controller further retrieves from the register storage each inversion bit associated with a transferred data stream and is operable to concurrently transfer the transferred data stream from the temporary storage and invert the bits associated with the transferred data stream if the inversion bit is set (col. 18, lines 29 – 56).

26. With respect to claim 25, Norman discloses a system for transferring a data stream, comprising:

- a control buffer (figure 3, 132, or accumulator register);

- a storage buffer (figure 3, 104);

- an inversion storage (figure 3, 118);

- a counting set of executable instructions to count set bits associated with a data stream being received from the control buffer directly into the storage buffer, wherein the control buffer (figure 7, 401) is an external data source to the storage buffer, and the counting set of executable instructions generates an inversion bit associated with the data stream, wherein the inversion bit is housed in the inversion storage and is set if a total number of set bits exceeds more than half a total number of bits associated with the data stream (abstract), and wherein the inversion storage, the storage buffer, and the counting set of instructions reside within the same controller and the device that is different from the another device associated with control buffer that supplies the data stream (figure 3).

27. With respect to claim 26, the system further comprises:

- a transfer set of executable instructions operable to use the counting set of executable instructions to transfer the data stream from the storage buffer to a target device, wherein the entire data stream is inverted if the inversion bit is set as the data stream is being transferred to the target device (col. 18, lines 29 – 56).

Art Unit: 2189

28. With respect to claims 40 and 41, Norman discloses a flash memory device (figure 3), comprising:

a temporary storage (104);

a receiving controller(102);

a counting controller (claim 24, col. 26, lines 26 – 34); and

a transferring controller that transfers a data packet directly received by the receiving controller in a temporary storage to an external target device and further inverts the data packet during the transfer if the counting controller indicates to the transferring controller that the packet requires inversion (claims 24 and 25, col. 26, lines 40 – 53), and wherein the counting controller and the temporary storage reside within the transferring controller (see figure 3).

29. With respect to claim 44, the counting controller includes a packet based ones counter (col. 13, line 45 – col. 19, line 64).

30. With respect to claim 45, the device further comprises a shift-load register (figure 3, 118) used to house an inversion bit generated by the counting controller, wherein the inversion bit, if set, indicates the data packet is to be inverted.

31. With respect to claim 46, one or more multiplexors (Figure 3, 106), the shift-load register (118), and the temporary storage (104) are used by the transferring controller to transfer the data packet.

Claim Rejections - 35 USC § 103

32. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

33. Claims 38, 42 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Norman in view of Goldstein (US Patent Application Publication No. 2003/0028672).

Norman discloses all of the limitations of the parent claims as discussed above. However, Norman does not specifically disclose specific applications of his inventions in a digital camera system that uses a compact flash memory. Variable size packet is not disclosed by Norman either. On the other hand, Goldstein discloses a digital camera system (figure 2A) and Compact Flash card (page 1, paragraph 4). Goldstein also discloses a variable packet size (page 2, paragraph 21).

It would have been obvious to one of ordinary skill in the art, having the teachings of Goldstein and Norman before him at the time the invention was made, to use the flash memory resource management teachings of Goldstein in the memory system of Norman, in order to provide memory management for electronic devices having limited and/or finite memory resources (Goldstein, page 1, paragraph 7).

Alternatively, it would also have been obvious to one of ordinary skill in the art, having the teachings of Goldstein and Norman before him at the time the invention was made, to use the bit inversion teachings of the flash memory system of Normal in the digital camera system of Goldstein, in order to reduce power consumption (col. 7, lines 1 – 4), reduce average time to write (col. 7, 37 – 39), and to increase the average life time of the array's cells (col. 7, lines 39 – 40).

Response to Amendment

34. Claim 25 has been amended to overcome a rejection under 35 USC 112, 2nd paragraph. Corresponding rejection of claims 25 is withdrawn.

Response to Arguments

35. Applicant's arguments filed November 2, 2006, have been fully considered but they are not persuasive. Contrary to Applicant's assertions, each device in la Iglesia and Norman, has its own storage and processing capabilities as shown above.

Conclusion

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

Art Unit: 2189

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Woo H. Choi
February 15, 2007